REMARKS/ARGUMENTS

1. Rejection of claims 2-3 under 35 U.S.C. 112, first paragraph:

Claims 2-3 are cancelled.

2. Rejection of claims 1-15 under 35 U.S.C. 112, second paragraph:

Claims 1 and 10 have been amended to overcome this rejection. Specifically, In claim 1, the relevant recitations "stopping on the polysilicon layer" and "etching ... a portion of the polysilicon layer, and stopping etching on the polysilicon layer" have been replaced with the expression "patterning the cap layer and the silicide layer to form a first stacked gate structure". In claim 10, the relevant recitations "stopping on the polysilicon layer" and "etching ... a portion of the polysilicon layer, and stopping etching on the polysilicon layer" have been replaced with the expression "patterning the cap layer and the silicide layer to form a first stacked gate structure using the patterned mask layer as a mask". These amendments find support in Fig.5 through Fig.10 for instance, and no new matter is entered. In addition, claims 2-3 have been cancelled, and claims 4-9 and 11-15 are respectively dependent on claims 1 and 10. Therefore, reconsideration of claims 1 and 4-15 is therefore respectfully requested.

3. Rejection of claims 1-3 and 6-9 under 35 U.S.C. 103(a) as being unpatentable over Liaw (US 6,448,140B1) in view of Gocho (US 6,258,654B1):

Claim 1 has been amended to overcome this rejection. Specifically, the

limitation "filling a passivation layer into the recess to form a second stacked gate structure, and removing the polysilicon layer and the gate oxide layer using the second stacked gate structure as a mask" is added to claim 1. This limitation finds support in Fig.5 through Fig.10 for instance, and no new matter is entered. The amended claim 1 is listed below for reference.

Claim 1 (currently amended). A method of forming a gate structure comprising:

providing a substrate, and consecutively forming a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer onto the substrate;

patterning the cap layer and the silicide layer to form a first stacked gate structure;

removing a portion of the silicide layer exposed on sidewalls of the first stacked gate structure for forming a recess on the sidewalls of the first stacked gate structure;

filling a passivation layer into the recess to form a second stacked gate structure; and

removing the polysilicon layer and the gate oxide layer using the second stacked gate structure as a mask.

Regarding US 6,448,140B1, Liaw discloses a method of forming a MOSFET device. Liaw teaches forming a gate insulating layer 2, a polysilicon layer 3, a tungsten silicide layer 4, and a capping layer 5, and etching these layer to form a gate structure (Fig.1). Liaw further teaches forming lateral recess 8 in the tungsten silicide layer 4 (Figs.2-3), and thermally growing a thick silicon oxide component 9c on the sides of the lateral recess 8.

Regarding US 6,258,654B1, Gocho discloses a method of manufacturing a semiconductor device. Gocho teaches etching a tungsten silicide layer and a polysilicon layer of a gate structure in two steps.

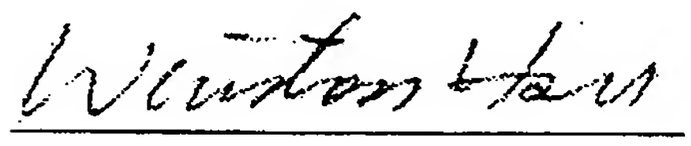
The examiner asserts that it would have been obvious to those skilled in the art to have used the two-step etch taught by Gocho in the process taught by Liaw. However, the applicant disagrees with that for the following reason. Liaw teaches forming a lateral recess 8 in the tungsten silicide layer 4, but the lateral recess 8 is formed while the tungsten silicide layer 4 and the polysilicon layer 3 are both etched. Consequently, when etching the tungsten silicide layer 4, the gate insulating layer 2 will be damaged. As for Gocho's teaching, although a two-step etching method is applied to form the gate structure, the gate structure of Cocho does not contain a recessed structure. Obviously, neither Liaw nor Gocho has expected that the polysilicon layer is able to protect the gate insulating layer when forming the recess. On the other hand, the removal of the silicide layer and the polysilicon layer in accordance with claim 1 is carried out in two steps. Specifically, the salicide layer is patterned using the first stacked gate structure as a mask, and the polysilicon layer is removed using the second stacked gate structure as a mask after the recess is formed. Therefore, the gate oxide layer would not be damaged when forming the recess. Since none of the cited arts teaches or suggests removing the polysilicon layer using the second stacked gate structure as a mask, the method of claim 1 has an unexpected result and it would not have been obvious to those skilled in the art to implement the method of claim1 in view of Liaw and Gocho. Claims 2-3 have been cancelled. Claims 6-9 are dependent on claim 1, and should be allowed if claim 1 is found

allowable Reconsideration of claims 1 and 6-9 is therefore respectfully requested.

Claims 4-5 are dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claims 4-5 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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